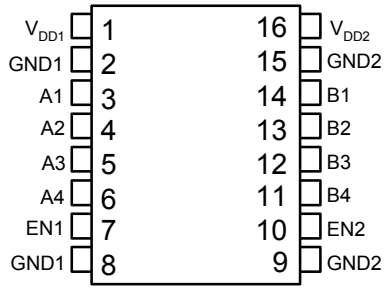
QUAD-CHANNEL DIGITAL ISOLATOR

Features

- High-speed operation: DC – 150 Mbps
- Low propagation delay: <10 ns
- Wide Operating Supply Voltage: 2.375–5.5 V
- Low power: I1 + I2 < 12 mA/channel at 100 Mbps
- Precise timing:
  2 ns pulse width distortion
  1 ns channel-channel matching
  2 ns pulse width skew
- 2500 V_{RMS} isolation
- Transient Immunity: >25 kV/µs
- Tri-state outputs with ENABLE control
- DC correct
- No start-up initialization required
- <10 µs Startup Time
- High temperature operation:
  125 °C at 100 Mbps
  100 °C at 150 Mbps
- Wide body SOIC-16 package

Pin Assignments

Wide Body SOIC



Top View

Applications

- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power factor correction systems

Safety Regulatory Approvals

- UL recognition:2500 V_{RMS} for 1 Minute per UL1577
- CSA component acceptance notice #5A
- ** All Pending*
- VDE certification conformity
  - DIN EN 60747-5-2 (VDE0884 Part 2):2003-01
  - DIN EN60950(VDE0805): 2001-12;EN60950:2000
  - V_{IORM} = 560 V_{PEAK}

Description

Silicon Lab's family of digital isolators are CMOS devices that employ an RF coupler to transmit digital information across an isolation barrier. Very high speed operation at low power levels is achieved. These parts are available in a 16-pin wide body SOIC package. Three speed grade options (1, 10, 100 Mbps) are available and achieve typical propagation delay of less than 10 ns.

Block Diagram

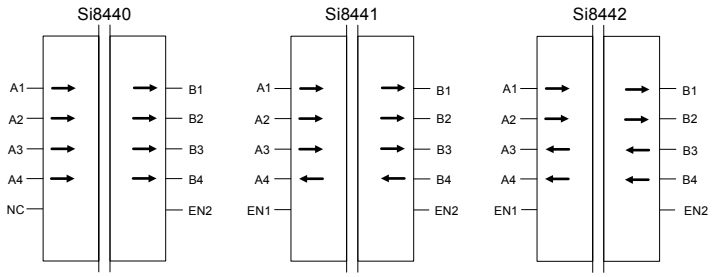


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Table 1. Electrical Characteristics
(V_{DD1} = 5 V, V_{DD2} = 5 V, T_A = –40 to 125 C°)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	μA
DC Supply Current (All inputs 0 V or at Supply)						
Si8440-A,-B,-C, V_{DD1}		All inputs 0 DC	—	7.5	—	mA
Si8440-A,-B,-C, V_{DD2}		All inputs 0 DC	—	7	—	mA
Si8440-A,-B,-C, V_{DD1}		All inputs 1 DC	—	15	—	mA
Si8440-A,-B,-C, V_{DD2}		All inputs 1 DC	—	6.5	—	mA
Si8441-A,-B,-C, V_{DD1}		All inputs 0 DC	—	8.7	—	mA
Si8441-A,-B,-C, V_{DD2}		All inputs 0 DC	—	11	—	mA
Si8441-A,-B,-C, V_{DD1}		All inputs 1 DC	—	14	—	mA
Si8441-A,-B,-C, V_{DD2}		All inputs 1 DC	—	12.5	—	mA
Si8442-A,-B,-C, V_{DD1}		All inputs 0 DC	—	10	—	mA
Si8442-A,-B,-C, V_{DD2}		All inputs 0 DC	—	10	—	mA
Si8442-A,-B,-C, V_{DD1}		All inputs 1 DC	—	13	—	mA
Si8442-A,-B,-C, V_{DD2}		All inputs 1 DC	—	13	—	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8440-B,-C, V_{DD1}			—	11	—	mA
Si8440-B,-C, V_{DD2}			—	9	—	mA
Si8441-B,-C, V_{DD1}			—	12	—	mA
Si8441-B,-C, V_{DD2}			—	13.5	—	mA
Si8442-B,-C, V_{DD1}			—	12.5	—	mA
Si8442-B,-C, V_{DD2}			—	12.5	—	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8440-C, V_{DD1}			—	12	—	mA
Si8440-C, V_{DD2}			—	27	—	mA
Si8441-C, V_{DD1}			—	16	—	mA
Si8441-C, V_{DD2}			—	27	—	mA
Si8442-C, V_{DD1}			—	21	—	mA
Si8442-C, V_{DD2}			—	21	—	mA

Table 1. Electrical Characteristics (Continued)
(V_{DD1} = 5 V, V_{DD2} = 5 V, T_A = –40 to 125 C°)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Maximum Data Rate			0	—	100	Mbps
Minimum Pulse Width			—	5	—	ns
Propagation Delay[1]	t_{PHL}, t_{PLH}		—	7.5	—	ns
Pulse Width Distortion[1]	PWD		—	1	—	ns
Propagation Delay Skew $\lvert t_{PLH} - t_{PHL} \rvert$[2]	t_{PSK}		—	6	—	ns
Channel-Channel Skew[3]	$t_{PSKCD/OD}$		—	0.5	—	ns
Output Rise Time		C1 = 15 pF	—	2	—	ns
Output Fall Time		C1 = 15 pF	—	2	—	ns
Common Mode Transient Immunity at Logic Low Output[4]	CM_L		—	30	—	kV/µs
Common Mode Transient Immunity at Logic High Output[4]	CM_H		—	30	—	kV/µs
Enable to Data Valid	t_{en1}		—	5	—	ns
Enable to Data Tri-State	t_{en2}		—	5	—	ns

Notes:
1. t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
2. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
3. Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
4. CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

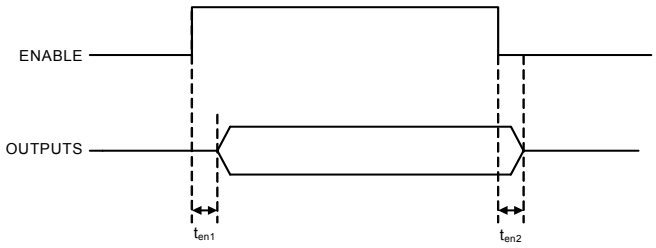


Figure 1. ENABLE Timing Diagram

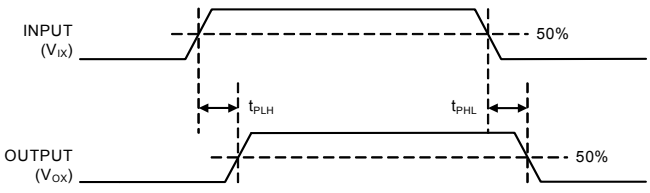


Figure 2. Propagation Delay Timing

Table 2. Electrical Characteristics
(V_{DD1} = 3.3 V, V_{DD2} = 3.3 V, T_A = –40 to 125 C°)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8440-A,-B,-C, V_{DD1}		All inputs 0 DC	—	7.3	—	mA
Si8440-A,-B,-C, V_{DD2}		All inputs 0 DC	—	6.5	—	mA
Si8440-A,-B,-C, V_{DD1}		All inputs 1 DC	—	14.3	—	mA
Si8440-A,-B,-C, V_{DD2}		All inputs 1 DC	—	6	—	mA
Si8441-A,-B,-C, V_{DD1}		All inputs 0 DC	—	8.3	—	mA
Si8441-A,-B,-C, V_{DD2}		All inputs 0 DC	—	10.8	—	mA
Si8441-A,-B,-C, V_{DD1}		All inputs 1 DC	—	13.3	—	mA
Si8441-A,-B,-C, V_{DD2}		All inputs 1 DC	—	11.8	—	mA
Si8442-A,-B,-C, V_{DD1}		All inputs 0 DC	—	9	—	mA
Si8442-A,-B,-C, V_{DD2}		All inputs 0 DC	—	9	—	mA
Si8442-A,-B,-C, V_{DD1}		All inputs 1 DC	—	12	—	mA
Si8442-A,-B,-C, V_{DD2}		All inputs 1 DC	—	12	—	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8440-B,-C, V_{DD1}			—	11	—	mA
Si8440-B,-C, V_{DD2}			—	8	—	mA
Si8441-B,-C, V_{DD1}			—	11.4	—	mA
Si8441-B,-C, V_{DD2}			—	14.5	—	mA
Si8442-B,-C, V_{DD1}			—	11.5	—	mA
Si8442-B,-C, V_{DD2}			—	11.5	—	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8440-C, V_{DD1}			—	11.4	—	mA
Si8440-C, V_{DD2}			—	18	—	mA
Si8441-C, V_{DD1}			—	12.5	—	mA
Si8441-C, V_{DD2}			—	21	—	mA
Si8442-C, V_{DD1}			—	17.5	—	mA
Si8442-C, V_{DD2}			—	17.5	—	mA

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V, V_{DD2} = 3.3 V, T_A = –40 to 125 C°)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Maximum Data Rate			0	—	100	Mbps
Minimum Pulse Width			—	5	—	ns
Propagation Delay[1]	t_{PHL},t_{PLH}		—	7.5	—	ns
Pulse Width Distortion[1]	PWD		—	1	—	ns
Propagation Delay Skew $\lvert t_{PLH} - t_{PHL} \rvert$[2]	t_{PSK}		—	8	—	ns
Channel-Channel Skew[3]	$t_{PSKCD/OD}$		—	1	—	ns
Output Rise Time		C1 = 15 pF	—	2	—	ns
Output Fall Time		C1 = 15 pF	—	2	—	ns
Common Mode Transient Immunity at Logic Low Output[4]	CM_L		—	30	—	kV/µs
Common Mode Transient Immunity at Logic High Output[4]	CM_H		—	30	—	kV/µs
Enable to Data Valid	t_{en1}		—	5	—	ns
Enable to Data Tri-State	t_{en2}		—	5	—	ns

Notes:

1. t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
2. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
3. Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
4. CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

Table 3. Electrical Characteristics
(V_{DD1} = 2.5 V, V_{DD2} = 2.5 V, T_A = –40 to 100 C°)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8440-A,-B,-C, V_{DD1}		All inputs 0 DC	—	6.8	—	mA
Si8440-A,-B,-C, V_{DD2}		All inputs 0 DC	—	6.3	—	mA
Si8440-A,-B,-C, V_{DD1}		All inputs 1 DC	—	12.5	—	mA
Si8440-A,-B,-C, V_{DD2}		All inputs 1 DC	—	5.8	—	mA
Si8441-A,-B,-C, V_{DD1}		All inputs 0 DC	—	7.8	—	mA
Si8441-A,-B,-C, V_{DD2}		All inputs 0 DC	—	9.8	—	mA
Si8441-A,-B,-C, V_{DD1}		All inputs 1 DC	—	12.5	—	mA
Si8441-A,-B,-C, V_{DD2}		All inputs 1 DC	—	11	—	mA
Si8442-A,-B,-C, V_{DD1}		All inputs 0 DC	—	8.8	—	mA
Si8442-A,-B,-C, V_{DD2}		All inputs 0 DC	—	8.5	—	mA
Si8442-A,-B,-C, V_{DD1}		All inputs 1 DC	—	11.5	—	mA
Si8442-A,-B,-C, V_{DD2}		All inputs 1 DC	—	11.5	—	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8440-B,-C, V_{DD1}			—	10.2	—	mA
Si8440-B,-C, V_{DD2}			—	7	—	mA
Si8441-B,-C, V_{DD1}			—	10.5	—	mA
Si8441-B,-C, V_{DD2}			—	11.5	—	mA
Si8442-B,-C, V_{DD1}			—	11	—	mA
Si8442-B,-C, V_{DD2}			—	11	—	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8440-C, V_{DD1}			—	10.8	—	mA
Si8440-C, V_{DD2}			—	14.5	—	mA
Si8441-C, V_{DD1}			—	12.5	—	mA
Si8441-C, V_{DD2}			—	17	—	mA
Si8442-C, V_{DD1}			—	15	—	mA
Si8442-C, V_{DD2}			—	15	—	mA

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V, V_{DD2} = 2.5 V, T_A = –40 to 100 C°)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Maximum Data Rate			0	—	100	Mbps
Minimum Pulse Width			—	5	—	ns
Propagation Delay[1]	t_{PHL},t_{PLH}		—	12	—	ns
Pulse Width Distortion[1]	PWD		—	1.5	—	ns
Propagation Delay Skew $\lvert t_{PLH} - t_{PHL} \rvert$[2]	t_{PSK}		—	10	—	ns
Channel-Channel Skew[3]	$t_{PSKCD/OD}$		—	1	—	ns
Output Rise Time		C1 = 15 pF	—	2	—	ns
Output Fall Time		C1 = 15 pF	—	2	—	ns
Common Mode Transient Immunity at Logic Low Output[4]	CM_L		—	30	—	kV/µs
Common Mode Transient Immunity at Logic High Output[4]	CM_H		—	30	—	kV/µs
Enable to Data Valid	t_{en1}		—	5	—	ns
Enable to Data Tri-State	t_{en2}		—	5	—	ns

Notes:

1. t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
2. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
3. Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
4. CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	100 Mbps, 15 pF, 5 V	–40	25	125	ºC
		150 Mbps, 15 pF, 5 V	0	25	100	ºC
Supply Voltage	V_{DD1}		2.375	—	5.5	V
	V_{DD2}		2.375	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{STG}	–65	—	150	ºC
Ambient Temperature Under Bias	T_A	–40	—	125	ºC
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	6	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	L_O	—	—	10	mA
Lead Solder Temperature (10s)		—	—	260	ºC
Maximum Isolation Voltage		—	—	4000	V_{DC}

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Package Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resistance (Input-Output)[1]	R_{IO}		—	10^{12}	—	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	—	1.4	—	pF
Input Capacitance[2]	C_I		—	4.0	—	pF
IC Junction-to-Case Thermal Resistance, Side 1	θ_{JCI}	Thermocouple located at center of package underside	—	33	—	ºC/W
IC Junction-to-Case Thermal Resistance, Side 2	θ_{JCO}		—	28	—	ºC/W

Notes:
1. Device considered a 2-terminal device; Pins 1– 8 shorted together and pins 9–16 shorted together.
2. Input capacitance is from any input data pin to ground.

Table 7. Regulatory Information

The Si84xx have been approved by the organizations listed below.

UL[1]	CSA	VDE[2]
Recognized under 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01[2]
Basic insulation, 2500 V RMS isolation voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V RMS maximum working voltage	Basic insulation, 560 V peak
		Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950:2000 Reinforced insulation, 560 V peak
File E257455	File 2500035643	File 5006301-4880-0001

Notes:

1. In accordance with UL1577, each Si84xx is proof tested by applying an insulation test voltage ≥ 3000 V RMS for 1 second (current leakage detection limit = 5 µA).
2. In accordance with DIN EN 60747-5-2, each Si84xx is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). A "*" mark branded on the component designates DIN EN 60747-5-2 approval.

Table 8. Insulation and Safety-related Specifications

Parameter	Symbol	Test Condition	Value	Unit
Rated Dielectric Insulation Voltage		1 minute duration	2500	V_{RMS}
Minimum External Air Gap (Clearance)	L(IO1)	Measured from input terminals to output terminals, shortest distance through air	7.7 min	mm
Minimum External Tracking (Creepage)	L(IO2)	Measured from input terminals to output terminals, shortest distance path along body	8.1	mm
Minimum Internal Gap (Internal Clearance)		Insulation distance through insulation	0.017 min	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 112/VDE 0303 Part 1	>175	V
Basic Isolation Group		Material Group (DIN VDE 0110, 1/89, Table 1)	IIIa	

Table 9. DIN EN 60747-5-2 (VDE 0884 Part 2) Insulation Characteristics[1,2]

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltages ≤ 150 V_{RMS} For Rated Mains Voltages ≤ 300 V_{RMS} For Rated Mains Voltages ≤ 400 V_{RMS}		 I-IV I-III I-II	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	V_{PEAK}
Input to Output Test Voltage, Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	V_{PR}	1050	V_{PEAK}
Input to Output Test Voltage, Method a After Environmental Tests Subgroup 1 (V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC) After Input and/or Safety Test Subgroup 2/3 (V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	 V_{PR} 	 896 672	 V_{PEAK} V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	4000	V_{PEAK}
Safety-Limiting Values (Maximum value allowed in the event of a failure; also see the thermal derating curve, Figure 3) Case Temperature Side 1 Current Side 2 Current	 T_S I_{S1} I_{S2}	 150 265 335	 ºC mA mA
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

Notes:
1. This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.
2. The * marking on packages denotes DIN EN 60747-5-2 approval for 560 V peak working voltage.

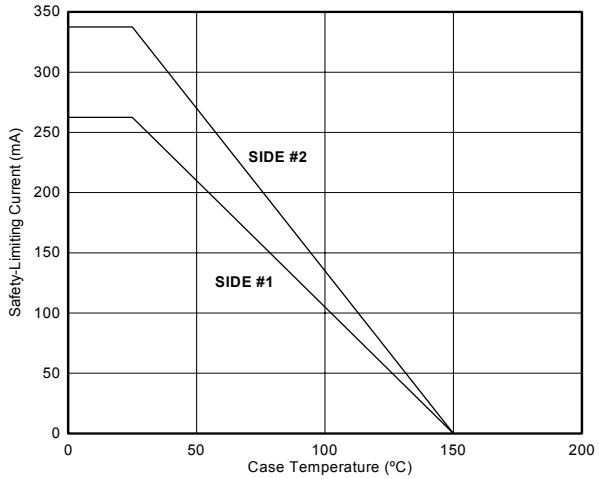


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Typical Performance Characteristics

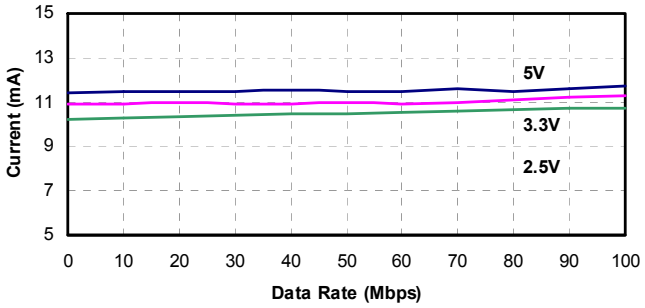


Figure 4. Si8440 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

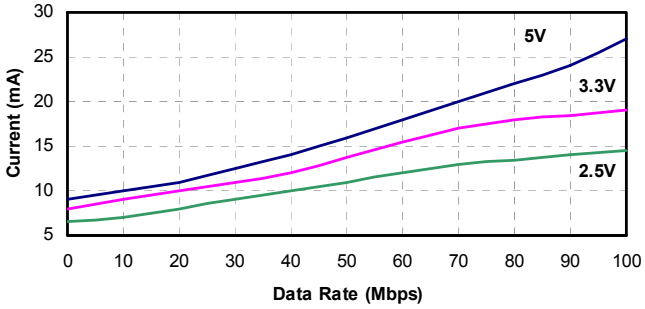


Figure 5. Si8440 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

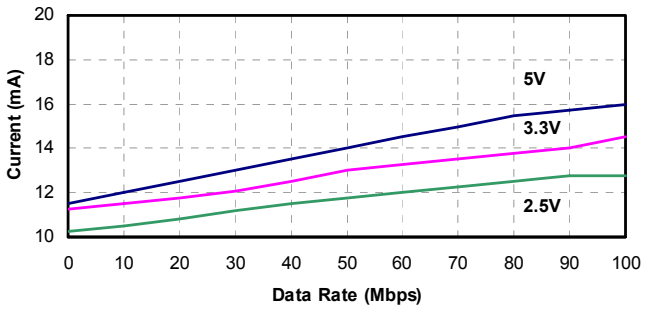


Figure 6. Si8441 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

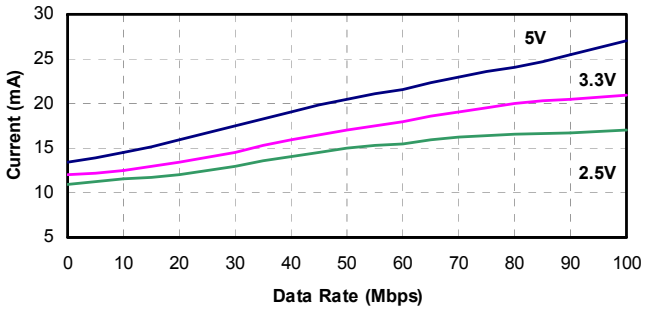


Figure 7. Si8441 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

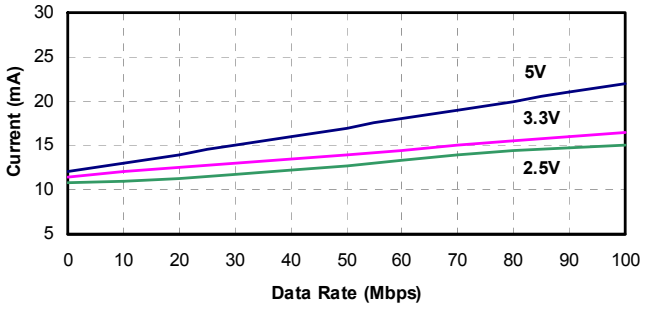


Figure 8. Si8442 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

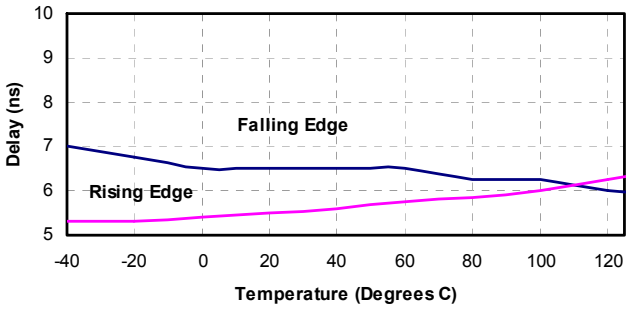


Figure 9. Propagation Delay vs. Temperature 5 V Operation

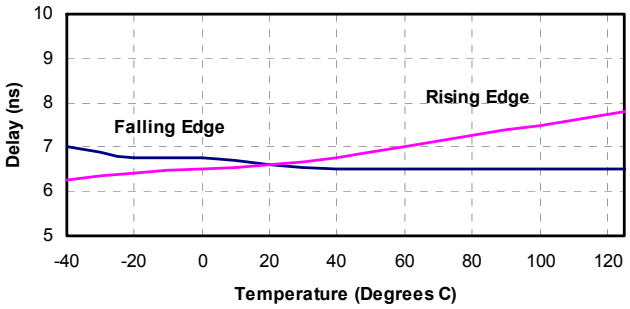


Figure 10. Propagation Delay vs. Temperature 3.3 V Operation

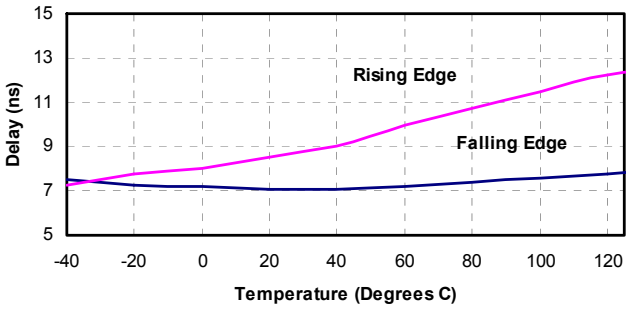


Figure 11. Propagation Delay vs. Temperature 2.5 V Operation

3. Application Information

3.1. Theory of Operation

The operation of an Si8440 channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si8440 channel is shown in Figure 12. A channel consists of an RF transmitter and receiver separated by a transformer.

Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying and applies the resulting waveform to the primary of the transformer. The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver.

3.2. Eye Diagram

Figure 13 illustrates an eye-diagram taken on an Si8440-IS. The test used an Anritsu (MP1763C) Pulse Pattern Generator for the data source. The output of the generator's clock and data from an Si8440-IS were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that very low pulse width distortion and very little jitter were exhibited.

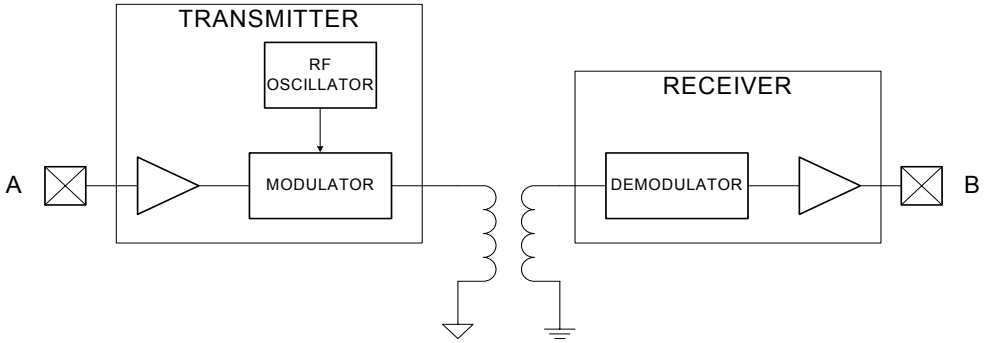


Figure 12. Simplified Channel Diagram

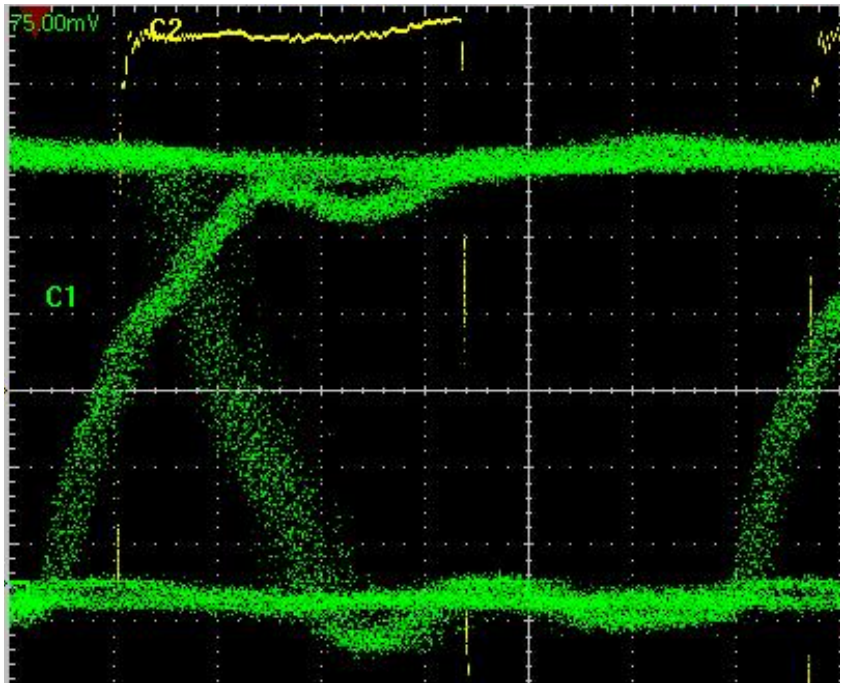


Figure 13. Eye Diagram

4. Layout Recommendations

Dielectric isolation is a set of specifications produced by the safety regulatory agencies from around the world that describes the physical construction of electrical equipment that derives power from a high-voltage power system such as 100–240 V_{AC} systems or industrial power systems. The dielectric test (or HIPOT test) given in the safety specifications places a very high voltage between the input power pins of a product and the user circuits and the user touchable surfaces of the product. For the IEC relating to products deriving their power from the 220–240 V power grids, the test voltage is 2500 V_{AC} (or 3750 V_{DC}—the peak equivalent voltage).

There are two terms described in the safety specifications:

- Creepage—the distance along the insulating surface an arc may travel.
- Clearance—the distance through the shortest path through air that an arc may travel.

Figure 14 illustrates the accepted method of providing the proper creepage distance along the surface. For a 220–240 V application, this distance is 8 mm and the wide body SOIC package must be used. There must be no copper traces within this 8 mm exclusion area, and the surface should have a conformal coating such as solder resist. The digital isolator chip must straddle this exclusion area.

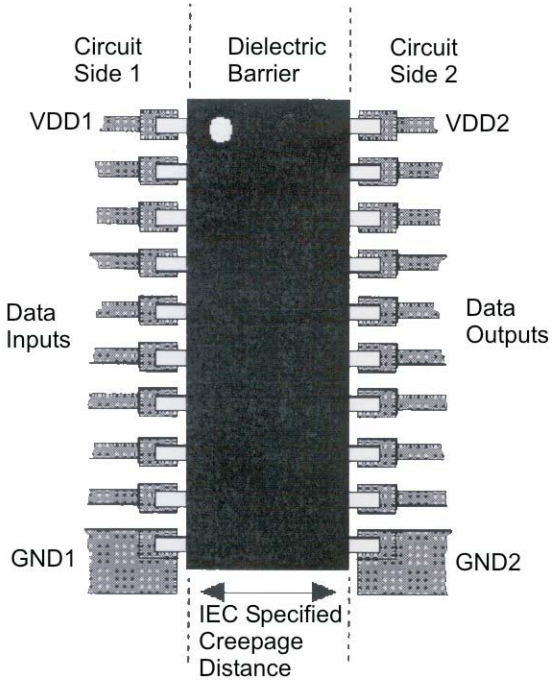


Figure 14. Creepage Distance

4.1. Supply Bypass

The Si8440 requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package.

4.2. Input and Output Characteristics

The Si8440 inputs and outputs are standard CMOS drivers/receivers.

4.3. Enable Inputs

The receiver output drivers are enabled when the Enable input is high and the drivers remain in a high-impedance state when Enable is low. The Enable input can be used for multiplexing or as a clock sync input. Supply currents remain at their nominal values when Enable is low.

4.4. RF Immunity and Common Mode Transient Immunity

The Si8440 family has very high common mode transient immunity while transmitting “0”s. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures up to 30 kV/µs. The Si844x has more susceptibility to common mode transients while transmitting “1”s, but meets 5 kV/µs and is typically 7.5 kV/µs. During a high surge event the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si844x family passes the industrial requirements of CISPR24 for RF immunity of 3 V/m using an unshielded evaluation board. As shown in Figure 15, the isolated ground planes form a parasitic dipole antenna, while Figure 16 shows the RMS common mode voltage versus frequency above which the Si844x becomes susceptible to data corruption. To avoid compromising data, care must be taken to keep RF common-mode voltage below the envelope specified in Figure 16. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

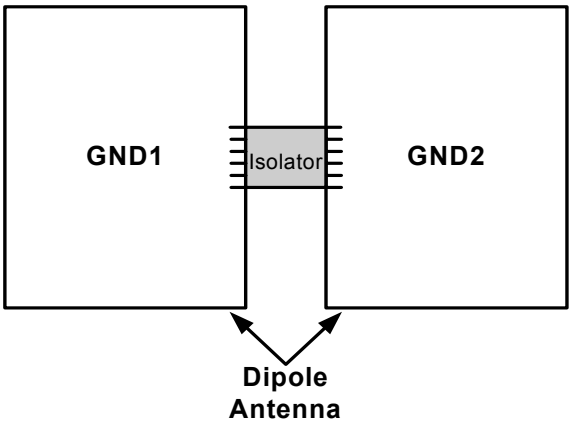


Figure 15. Dipole Antenna

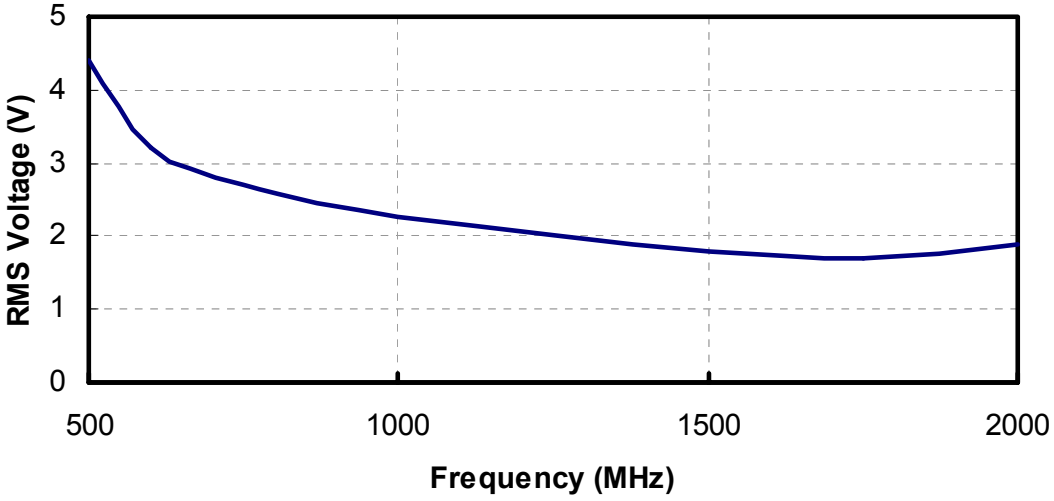


Figure 16. RMS Common Mode Voltage vs. Frequency

4.5. RF Radiated Emissions

The Si8440 family uses a RF carrier frequency of approximately 2.1 GHz. This will result in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC chip but due to a small amount of RF energy driving the isolated ground planes which can act as a dipole antenna.

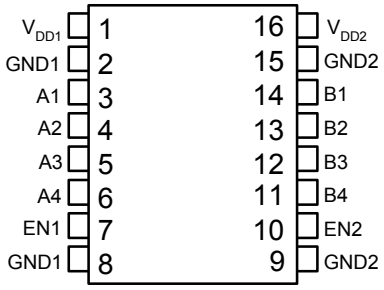
The unshielded Si8440 evaluation board passes FCC requirements. Table 10 shows measured emissions compared to FCC requirements.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

Table 10. Radiated Emissions

Frequency (GHz)	Measured (dBµV/m)	FCC Spec (dBµV/m)	Compared to Spec (dB)
2.094	70.0	74.0	–4.0
2.168	68.3	74.0	–5.7
4.210	61.9	74.0	–12.1
4.337	60.7	74.0	–13.3
6.315	58.3	74.0	–15.7
6.505	60.7	74.0	–13.3
8.672	45.6	74.0	–28.4

5. Pin Descriptions



Top View

Wide Body SOIC

Name	SOIC-16 Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital I/O	Side 1 digital input or output.
A4	6	Digital I/O	Side 1 digital input or output.
EN1	7	Digital Input	Side 1 active high enable. NC on Si8440.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2	10	Digital Input	Side 2 active high enable.
B4	11	Digital I/O	Side 2 digital input or output.
B3	12	Digital I/O	Side 2 digital input or output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.

6. Ordering Guide

Ordering Part Number	Number of Inputs V_{DD1} Side	Number of Inputs V_{DD2} Side	Maximum Data Rate	Temperature	Package Type
Si8440-A-IS	4	0	1	–40 to 125 °C	SOIC-16
Si8440-B-IS	4	0	10	–40 to 125 °C	SOIC-16
Si8440-C-IS	4	0	100	–40 to 125 °C	SOIC-16
Si8441-A-IS	3	1	1	–40 to 125 °C	SOIC-16
Si8441-B-IS	3	1	10	–40 to 125 °C	SOIC-16
Si8441-C-IS	3	1	100	–40 to 125 °C	SOIC-16
Si8442-A-IS	2	2	1	–40 to 125 °C	SOIC-16
Si8442-B-IS	2	2	10	–40 to 125 °C	SOIC-16
Si8442-C-IS	2	2	100	–40 to 125 °C	SOIC-16

Note: All packages Pb-free and RoHS compliant. Moisture sensitivity level is MSL2 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications, and peak solder temperature.

7. Package Outline: Wide Body SOIC

Figure 17 illustrates the package details for the Quad-Channel Digital Isolator. Table 14 lists the values for the dimensions shown in the illustration.

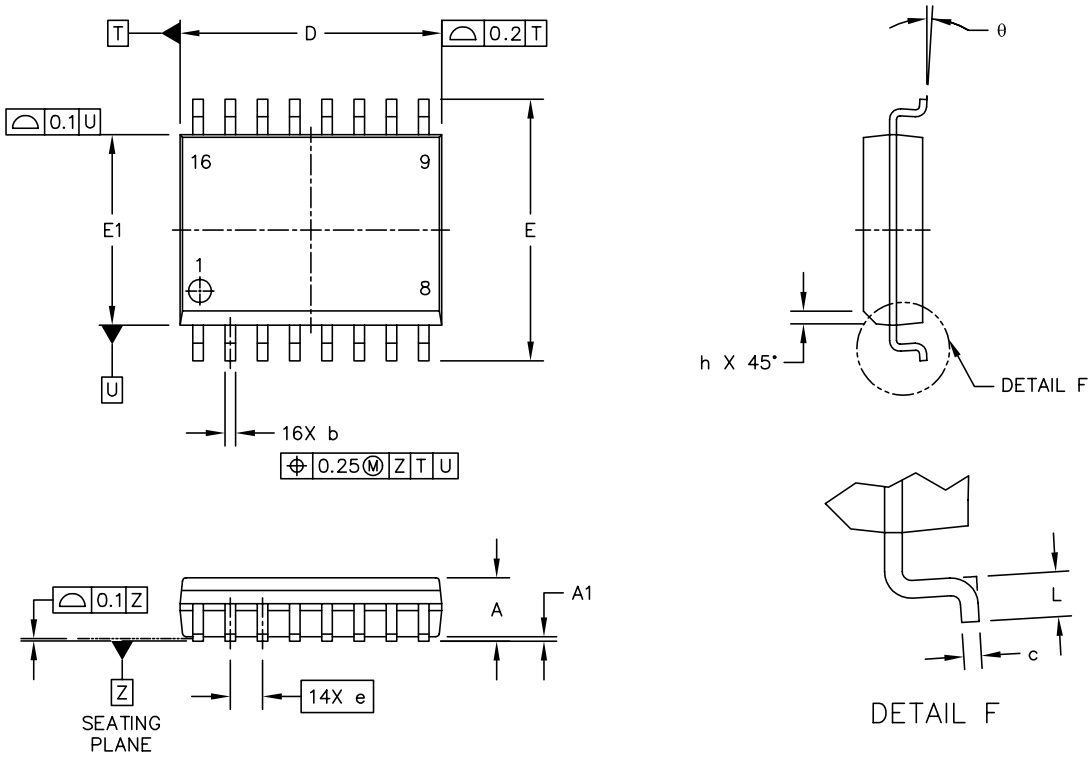


Figure 17. 16-Pin Wide Body SOIC

Table 14. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

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